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Thermal-fluid flow in parallel boards with heat generating blocks

Takahiro Furukawa, Wen-Jei Yang *

Department of Mechanical Engineering and Applied Mechanics, University of Michigan, 2250 G.G. Brown, Ann Arbor, MI 48109-2125, USA

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Abstract

A method is developed to numerically investigate thermal-fluid flow behavior in a bundle of parallel boards with heat producing blocks. The system simulates cooling passages in a stack of electronic circuit boards with heat generating chips. At a low Reynolds number flow, a developing flow may achieve a fully developed flow state at certain block number from the entrance. Thermal conductivity of the board and thermal contact resistance between the chip and board has a considerable impact on thermal performance. The fluid flow and heat transfer performance in this channel flow is similar to that in ribbed channel flow.

1. Introduction

One fetal shortcoming of electronic components and devices is a limit on operating temperature in order to ascertain their accuracy and reliability. With a trend in reducing their volume, heat generating density increases accordingly. As a result, thermal management of electronic equipment and devices has become a crucial problem in electronic industry. A number of studies on cooling of electronic devices were discussed by Nakayama [1] and Incropera [2]. Numerical simulation of laminar developing flow and heat transfer in two-dimensional ribbed channel has been performed by Davalath and Bayazitoglu [3] and Kim and Anand [4]. Periodically fully developed flow in a similar ribbed channel has been studied by Schmidt and Patankar [5] and Kim and Anand [6]. This study deals with numerical simulation of flow and heat transfer problem in a stack of two parallel boards with a series of ten heat generating blocks attached on the surface of one board. The system simulates cooling in a stack of circuit boards with heat generating chips. The study is unique in that both the velocity and temperature are in developing stage inside each channel. Both profiles may eventually achieve a fully developed stage at further downstream. Results show how friction factor and heat transfer performance (in the form of thermal resistance or heat transfer coefficient) evolve along the flow through the coolant channel. The results resemble those in ribbed channel flow with a distinct difference in that the former has heat generation in only the blocks while the latter has heating from both the blocks (ribs) and the board (primary surface). Some problems which are unique in electronic cooling, such as case-to-board thermal contact resistance, junction-to-case thermal resistance, and non-uniform conductivity of the board are also treated.

2. Formation of the problem

The physical system to be studied consists of a bundle of parallel plates with a series of heat generating blocks attached to one side of every other board surface. Since the heat generating blocks are placed on one side of the channel surfaces, one may define each channel enclosed by the midplanes of two adjacent boards S_1 and S_2 is defined as the control volume, as shown in Fig. 1, for theoretical analysis. A coolant flows through the bundle

* Corresponding author. Tel.: +1-734-995-4735.
E-mail address: wjyang@engin.umich.edu (W.-J. Yang).

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Nomenclature

B	block height, m
D	channel space, m
D_h	hydrodynamic diameter of channel, m
f	friction factor
h	heat transfer coefficient, W/m^2 K
H	fin height or height of a stack of boards, m
K	thermal conductivity, W/m K
L	channel length, m
N	total number of block
p	pressure, N/m^2
P	block pitch, m
Pe	Peclet number
Pr	Prandtl number
q	heat transfer rate, W
R	thermal resistance, K/W
R''	thermal contact resistance, m^2 K/W
Re	Reynolds number
R_{th}	thermal resistance between chip and channel bulk flow, K/W
R_ϕ	residual
S	block space, m
t	board thickness, m
T	temperature, K
T_∞	ambient temperature, K
u, v	velocity, m/s
V	inlet velocity of channel, m/s
W	heat sink width or block width, m
x, y	coordinate, m

Greek symbols

Δx	space between the chip case and board, m
ε	convergence criterion
ϕ	dependent variable

Superscripts

k	iteration number
-	dimensionless
$'$	per unit length
$''$	per unit square

Subscripts

a	air
ave	average
b	block or bulk
c	chip
cb	case-to-base
int	interface
i, j	x- and y-direction grid numbers
j	junction
jc	junction to case
l	local
max	maximum
nb	neighbor
pl	board in-plane
ref	reference
th	through board thickness

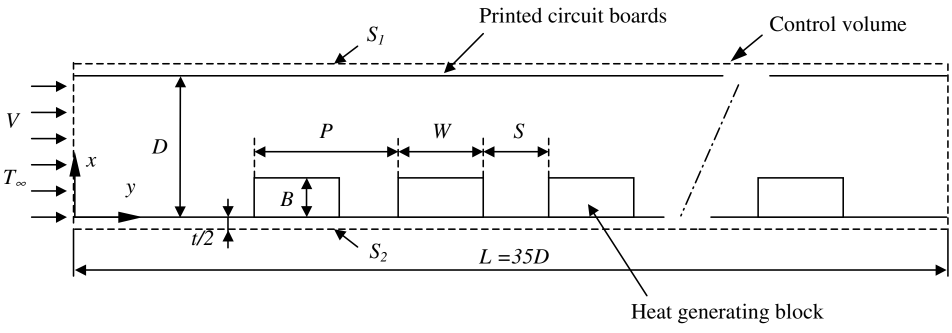


Fig. 1. A schematic of the physical system to be studied.

to remove the heat generated by the blocks. Thus, the system simulates cooling of a stack of electronic circuit boards with heat generating chips. The temperature field in each flow channel is thermally coupled with adjacent channels because heat transfer from the board to the coolant is by the conduction–convection conjugate mode. The origin of the coordinate system, x and y, is fixed at the entrance on the inner surface of the board S_2, with x measuring the distance in the transverse direction and y for the distance in the stream-wise direction. D denotes the channel width; L, the channel length; t, board thickness; B, block height; W, block width; S, distance between blocks; and P, pitch between blocks. Ten heat-generating blocks are modeled in the developing channel flow model. The entrance length between the inlet and first block is set to be $4W$ and the channel length is $35W$ in the model.

Let the flow through the channel be two-dimensional, steady and laminar. It enters the channel, at $y = 0$, with uniform velocity V and temperature T_∞. u and v are the velocity components in the x- and y-direction, respectively and T is the temperature at location (x, y). Let us define the dimensionless variables as

$$\bar{u} = \frac{u}{V}, \quad \bar{v} = \frac{v}{V}, \quad \bar{x} = \frac{x}{D}, \quad \bar{y} = \frac{y}{D},$$
$$\overline{W} = \frac{W}{D}, \quad \overline{B} = \frac{B}{D}, \quad \overline{T} = \frac{T - T_\infty}{q_b'/k_a} \tag{1}$$

where q_b' is the heat transfer rate from each block per unit length perpendicular to the xy plane and k_a is the average air thermal conductivity. Consideration is given to steady laminar incompressible airflow, and an assumption is imposed that all thermal properties of flow and solidity, including density, viscosity, and conductivities, are constant.

With neglect of viscous dissipation and gravity force, the governing differential equations in dimensionless form can be expressed as

Continuity

$$\frac{\partial \bar{u}}{\partial \bar{x}} + \frac{\partial \bar{v}}{\partial \bar{y}} = 0 \tag{2}$$

x-direction momentum

$$\bar{u}\frac{\partial \bar{u}}{\partial \bar{x}} + \bar{v}\frac{\partial \bar{u}}{\partial \bar{y}} + \frac{\partial \bar{p}}{\partial \bar{x}} = \frac{1}{Re}\left(\frac{\partial^2 \bar{u}}{\partial \bar{x}^2} + \frac{\partial^2 \bar{u}}{\partial \bar{y}^2}\right) \tag{3}$$

y-direction momentum

$$\bar{u}\frac{\partial \bar{v}}{\partial \bar{x}} + \bar{v}\frac{\partial \bar{v}}{\partial \bar{y}} + \frac{\partial \bar{p}}{\partial \bar{y}} = \frac{1}{Re}\left(\frac{\partial^2 \bar{v}}{\partial \bar{x}^2} + \frac{\partial^2 \bar{v}}{\partial \bar{y}^2}\right) \tag{4}$$

Energy

$$\bar{u}\frac{\partial \overline{T}}{\partial \bar{x}} + \bar{v}\frac{\partial \overline{T}}{\partial \bar{y}} = \frac{k/k_a}{Pe}\left(\frac{\partial^2 \overline{T}}{\partial \bar{x}^2} + \frac{\partial^2 \overline{T}}{\partial \bar{y}^2}\right) + \frac{f(\Omega)}{\overline{W}\overline{B}Pe} \tag{5}$$

Here, $f(\Omega)$ is a kronecker delta taking the value of unity in the block and zero in the fluid, that is,

$$f(\Omega) = \begin{cases} 1, & \text{in block} \\ 0, & \text{in fluid} \end{cases} \tag{6}$$

Note that the volume of the heat source, characterized by the product of the width and height of non-dimensionalized block, appears in the source term of the energy equation.

No-slip boundary conditions are applied at the two parallel plates and the block surface. Both the axial diffusion and pressure are set to be zero at the channel exit. The fluid is assumed to enter the channel with uniform velocity and temperature profiles. Then, the velocity boundary conditions become

$$\bar{u}, \bar{v} = 0 \quad \text{at the board and block surface} \tag{7}$$

$$\bar{u} = 0, \quad \bar{v} = 1 \quad \text{at } 0 < \bar{x} < 1 \text{ and } \bar{y} = 0 \tag{8}$$

$$\frac{\partial \bar{u}}{\partial \bar{y}} = 0, \quad \frac{\partial \bar{v}}{\partial \bar{y}} = 0 \quad \text{at } 0 < \bar{x} < 1 \text{ and } \bar{y} = L/D \tag{9}$$

In addition, the pressure at the channel exit is set to zero.

The thermal inlet and outlet boundary conditions

$$\overline{T} = 0 \quad \text{at } 0 < \bar{x} < 1, \ \bar{y} = 0 \tag{10}$$

$$\frac{\partial \overline{T}}{\partial \bar{y}} = 0 \quad \text{at } 0 < \bar{x} < 1, \ \bar{y} = L/D \tag{11}$$

Because of symmetrical arrangement of a stack of parallel boards, a repeated boundary condition may apply at the midplanes of the board S_1 and S_2 to simulate thermal coupling between two adjacent channels.

$$k_{b,th}\frac{\partial \overline{T}}{\partial \bar{x}}\bigg|_{(-\bar{t}/2,\bar{y})} = k_{b,th}\frac{\partial \overline{T}}{\partial \bar{x}}\bigg|_{(1+\bar{t}/2,\bar{y})} \tag{12}$$

$$\overline{T}_{(-\bar{t}/2,\bar{y})} = \overline{T}_{(1+\bar{t}/2,\bar{y})} \tag{13}$$

where $k_{b,th}$ is conductivity through the board thickness. The inlet temperature is set to equal the ambient temperature while the exit boundary is placed at the middle of the last block in the flow direction. To simulate infinitely repeated blocks in the stream-wise direction, the outlet thermal boundary conditions for both the fluid and solid temperature field can be described as

$$\left(\frac{\partial \overline{T}}{\partial \bar{y}}\right)_{\text{in the middle of } (N-1)\text{th block}} = \left(\frac{\partial \overline{T}}{\partial \bar{y}}\right)_{\text{in the middle of } N\text{th block}} \tag{14}$$

The above equation implies that temperature rise through the centerline of the $(N-1)$th block is the same as that at through the center line of the Nth block. Since ten heat generating blocks are considered in this developing channel flow, N is set to be 10 in this study.

3. Numerical solutions

A numerical procedure called SIMPLER [7] was used to solve the governing differential equations. The finite difference mesh consists of many rectangular control volumes forming a staggered grid system. Different control volumes are used for the x-, y-direction momentum and continuity equations. The discretized equations are constructed by means of a power law scheme. The flow field is solved by the line-by-line tridiagonal matrix algorithm (TDMA) [8,9]. This scheme is a combination of the direct method and the Gauss–Seidel method. Since the repeated conditions are applied to the temperature field in the transverse direction, the cyclic tri-diagonal matrix algorithm (CTDMA) [10] is used to sweep in the stream-wise direction.

Since the solution procedure is iterative, some criterion is used to determine the convergence of the solution. A residual R_ϕ defined as

$$R_\phi = \sqrt{\sum(a_{\text{nb}}\phi_{\text{nb}} + b_{i,j} - a_{i,j}\phi_{i,j})^2} \tag{15}$$

is used at each nodal point.

The first convergence criterion, ε_1, is set at

$$\varepsilon_1 = \frac{R_\phi}{R_{\phi,\text{ref}}} < 10^{-3} \tag{16}$$

where $R_{\phi,\text{ref}}$ denotes either the residual of the initial calculation or the maximum residual in the entire calculation. The second convergence criterion, ε_2, is defined as

$$\varepsilon_2 = \frac{\sum_{i,j}(\phi_{i,j}^{k+1} - \phi_{i,j}^{k})^2}{\sum_{i,j}(\phi_{i,j}^{k+1})^2} < 10^{-5} \tag{17}$$

for local values. Here, k is an iteration number. Convergence is achieved when both conditions are satisfied. ε_1 is larger than ε_2 in order to economize the computational time because ε_1 deals with convergence of the entire solution while ε_2 concerns with local values.

In order to accurately simulate heat transfer phenomena in electronic devices, it is essential to correctly model some physical quantities including the solid–fluid interfacial thermal conductivity k_{int}, junction-to-case thermal resistance R_{jc} and case-to-board thermal contact resistance R''_{cb}.

3.1. Solid–fluid interfacial thermal conductivity

Consider an interface between a solid phase Pe and a liquid phase eE of thickness $(\delta x)_{e-}$ and $(\delta x)_{e+}$, respectively. The plane e represents the solid–fluid interface. Let T_P, T_e and T_E be the temperatures at the planes P, e and E, respectively and k_P and k_E be the thermal conductivities of the solid and fluid phases, respectively. Then, the heat flux at the interface q''_e can be written as

$$q''_e = \frac{k_{\text{int}}(T_P - T_E)}{(\delta x)_e} = \frac{k_P(T_P - T_e)}{(\delta x)_{e-}} = \frac{k_E(T_e - T_E)}{(\delta x)_{e+}} \tag{18}$$

It yield the definition of the interfacial thermal conductivity as

$$k_{\text{int}} = \frac{k_E k_P}{k_E\frac{(\delta x)_{e-}}{(\delta x)_e} + k_P\frac{(\delta x)_{e+}}{(\delta x)_e}} \tag{19}$$

3.2. Thermal resistances

The ultimate goal in thermal management of electronic devices is to restrict the component junction temperature T_{j}, within its maximum allowable value specified by the manufacturer. Most often, chip manufacturers provide the junction-to-case thermal resistance R_{jc} for chips. The chip case is not directly placed on the board but instead it is connected to the board by the leads, thus creating an air space between the chip and the board Δx_{a}, as illustrated in Fig. 2. Hence, the case-to-board thermal resistance R''_{cb} may be modeled in the numerical simulation for determining the junction temperature. The thermal resistance R_{jc} and R''_{cb} are defined as

$$R_{\text{jc}} = \frac{T_{\text{j}} - T_{\text{c,top}}}{q_{\text{c}}} \quad \text{and} \quad R''_{\text{cb}} = \frac{T_{\text{c,bot}} - T_{\text{b}}}{q''_{\text{cb}}} \tag{20}$$

respectively. q_{c} is the total heat dissipation from the chip and q''_{cb} is the heat flux through the chip case and board. The quantities with double prime denote those per unit heat transfer area.

In the present study, the heat-generating block is mounted directly on the board and the air space is not modeled in numerical simulations. Instead of modeling the physical air space, thermal resistance can be assigned

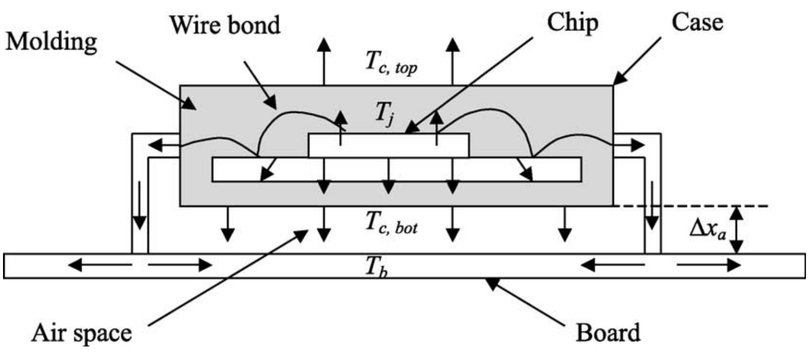


Fig. 2. Detail description and heat transfer path of an electronic component.

at the interface of the block and board. Thermal resistances can be modeled by modifying the interface conductivity of the board and block. It can be shown that [11]

$$R''_{\mathrm{cb}} = \frac{\Delta x_{\mathrm{a}}}{k_{\mathrm{a}}} \tag{21}$$

where Δx_{a} is the air space and k_{a} is the thermal conductivity of air. Therefore, the thermal contact resistance between the case and board is calculated by knowing the air gap thickness.

3.3. Thermal conductivity of printed circuit board

A typical printed circuit board is a layered composite material consisting of layers of copper foil and glass-reinforced polymer (FR-4). Due to low thermal conductivity of the FR-4 and absence of a continuous copper path, the thermal conductivity through the thickness of the plane $k_{\mathrm{b,th}}$ in the traverse direction is much lower than that within the plane $k_{\mathrm{b,pl}}$ in the streamwise direction. The magnitudes of $k_{\mathrm{b,pl}}$ and $k_{\mathrm{b,th}}$ in a typical PCB having two internal copper planes and two FR-4 layers are 17.4 and 0.26 W/m K, respectively [12]. Since the heat generated by a chip is dissipated through the PCB, these two thermal conductivities play an important role in lowering thermal resistance from the chip to the ambient. Low conductivity of $k_{\mathrm{b,th}}$ results in an increase in the thermal resistance. A remedy of low thermal conductivity can be achieved by installing a number of thermal vias or heat slugs in the transverse direction. The use of the thermal vias or heat slugs enhances heat dissipation form the chip component. Note that the thermal conductivities $k_{\mathrm{b,pl}}$ and $k_{\mathrm{b,th}}$ are employed in the present numerical simulation.

4. Results and discussion

The friction factor per module, f, is defined as

$$f = \frac{p(x,y) - p(x,y+P)}{P}\frac{D_{\mathrm{h}}}{\rho V^2/2} \tag{22}$$

Heat transfer performance is presented as the local and average heat transfer coefficients h_{l} and h_{ave}, respectively. First it is necessary to define a reference temperature. Moffat and Anderson [13] proposed a few options and finally selected adiabatic temperature as the reference temperature obtained from a superposition of the Kernel function. It can be used independently of flow and heating conditions but required the information at the inlet. Kim and Anand [4] selected bulk temperature T_{b} as the reference temperature, which is defined as

$$T_{\mathrm{b}} = \frac{\int_0^D |v| T \,\mathrm{d}x}{\int_0^D |v| \,\mathrm{d}x} \tag{23}$$

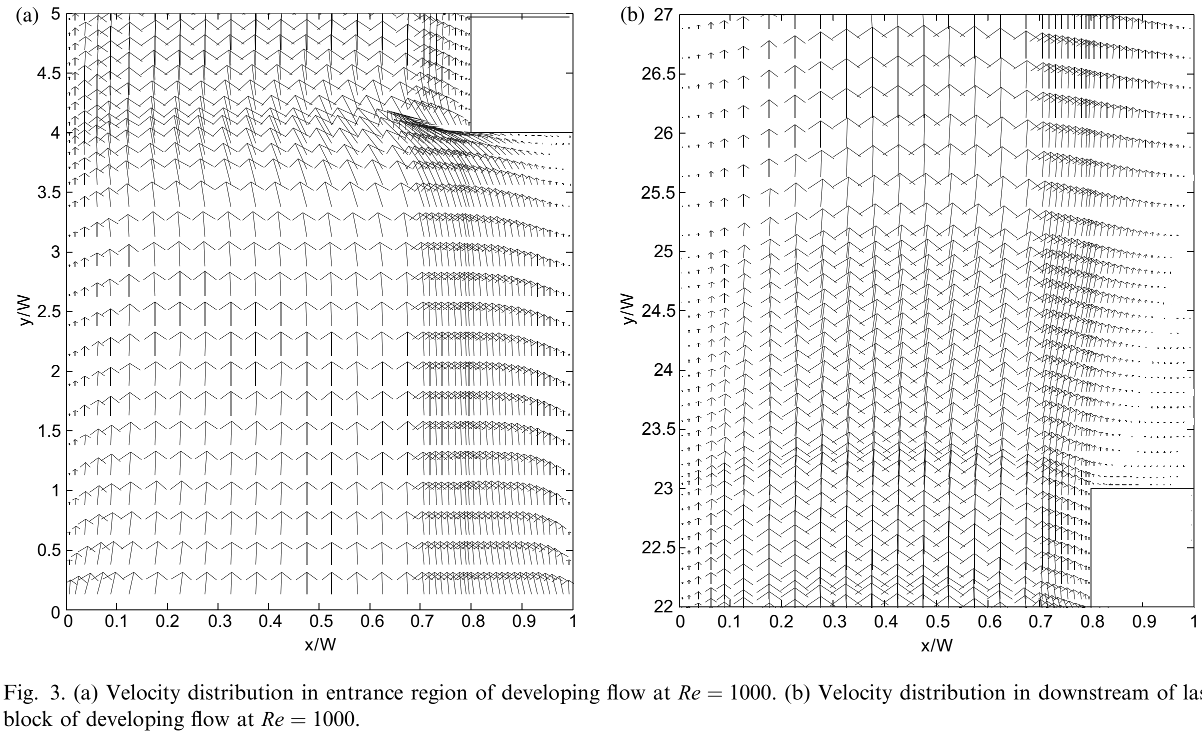


Fig. 3. (a) Velocity distribution in entrance region of developing flow at $Re = 1000$. (b) Velocity distribution in downstream of last block of developing flow at $Re = 1000$.

The bulk temperature can be easily obtained for both developing flow in channels and a periodically fully developed flow in modules. In this study, only constant heat source is treated. For such case, the bulk temperature is not affected by different upstream heating conditions. The local heat transfer coefficient of the channel flow is defined based on the bulk temperature and local surface temperature T_s as

$$h_l = \frac{-k_{\text{int}}\left(\frac{dT}{dy}\right)_{\text{at local surface}}}{T_s - T_b} \tag{24}$$

The heat transfer coefficient in the channel module may be used to compare the thermal performance for the developed flow and periodically fully developed flow. It is calculated along the upper board surface and top surface of the block. The average heat transfer coefficient is defined as

$$h_{\text{ave}} = \frac{1}{P+W}\left(\int_{\text{upper board}} h_l\,dy + \int_{\text{block top}} h_l\,dy\right) \tag{25}$$

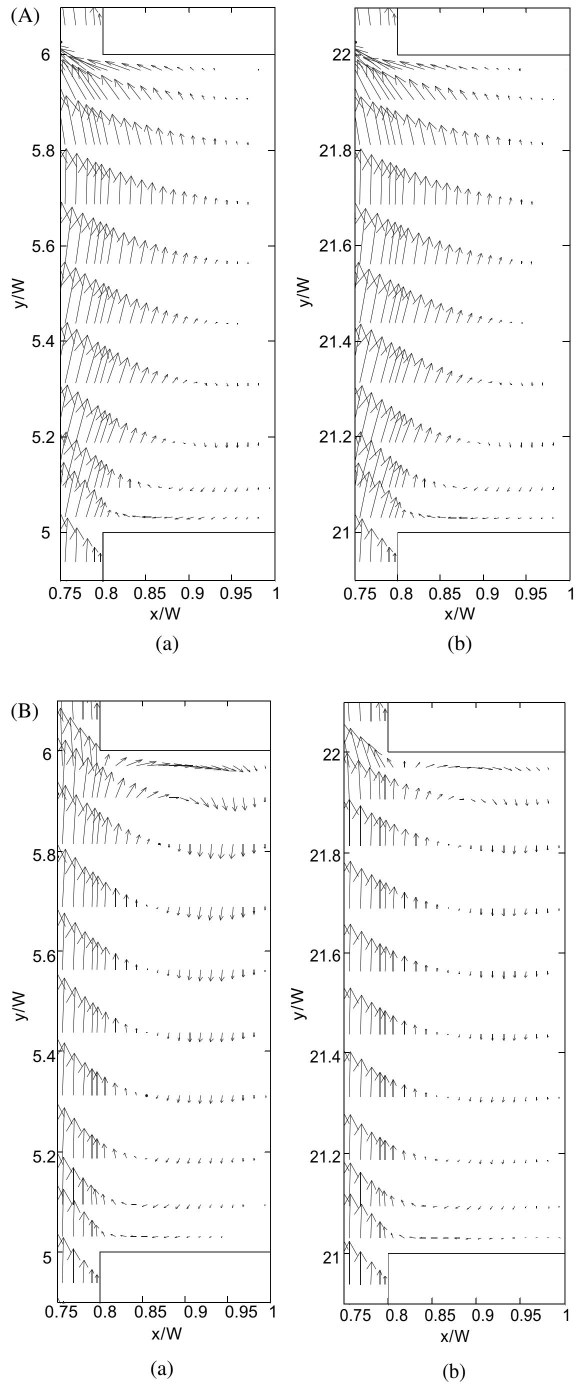


Fig. 4. Cavity flow in developing flow for $B/W = 0.2$ at $Re = 100$ (A) and $Re = 1000$ (B): (a) first cavity and (b) ninth cavity.

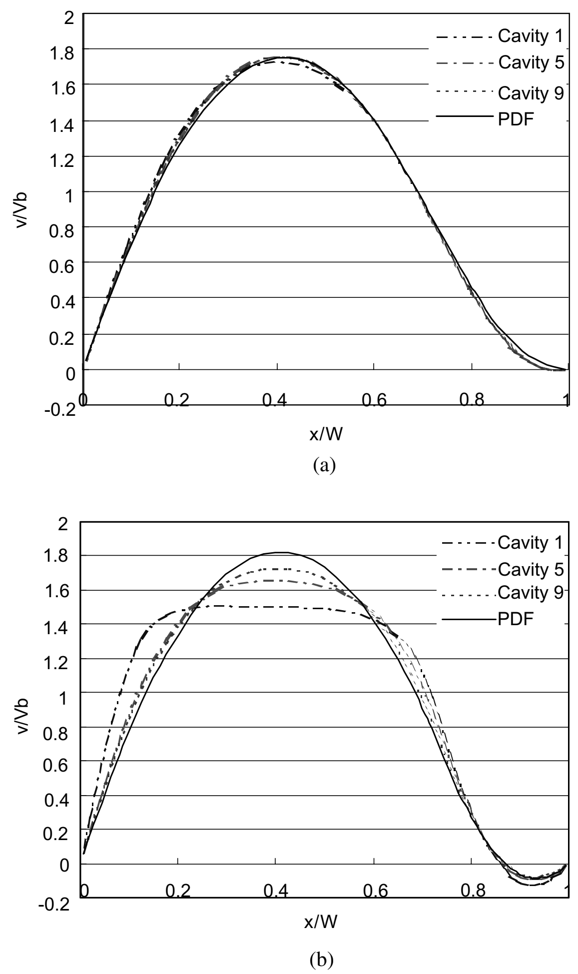


Fig. 5. Transverse velocity profiles at the middle of cavities, $B/W = 0.2$: (a) $Re = 100$ and (b) $Re = 1000$.

An alternative way of expressing heat transfer performance is through the use of thermal resistance between the chip and bulk channel flow which is defined as

$$R_{\mathrm{th}} = \frac{T_{\mathrm{c,max}} - T_{\mathrm{b}}}{q_{\mathrm{c}}} \tag{26}$$

Here, $T_{\mathrm{c,max}}$ is the maximum temperature of the block and its magnitude represents the junction temperature of the chip T_{j}. q_{c} denotes the heat generation rate from the block.

Results for velocity vectors, friction factor, isotherms, heat transfer coefficients, and thermal resistance are presented in Figs. 3–8.

4.1. Fluid flow behavior

Fig. 3(a) and (b) show the velocity-vector distributions in the entrance region and the region downstream from the last block, respectively, of a developing flow in the channel. The Reynolds number is at 1000. The entrance region refers to the flow regime from the inlet to the upstream end of the first block. It is observed that the incoming flow impacts on the first block, resulting in an abrupt change in its direction. Another special flow characteristic is a step-down flow in the wake region behind the downstream end of the last (10th) block. A flow circulation is observed in the wake region with the size of about a two-block length. It is of importance to note that flow patterns in Fig. 3(a) and (b) exhibit the characteristics of the up-step and down-step flow, respectively.

Fig. 4(A) and (B) show circulation flows in the first and ninth cavity at the Reynolds numbers of 100 and 1000, respectively. Notice the formation of a circulating flow in the wake region behind the upstream heating block in Fig. 4(A) at a low Reynolds number of 100. As

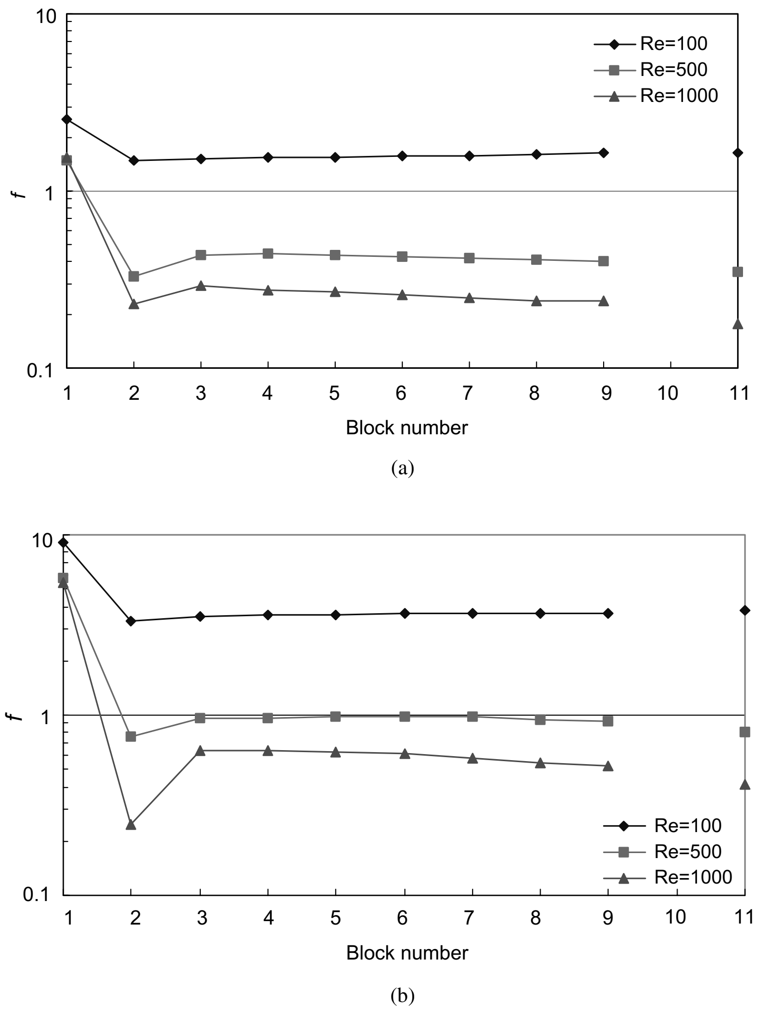


Fig. 6. Variation of friction factor in the stream-wise direction: (a) $B/W = 0.2$ and (b) $B/W = 0.4$.

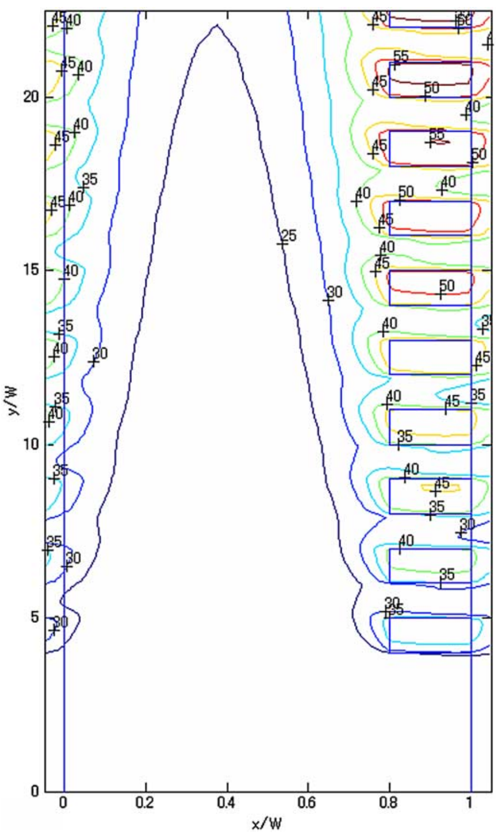


Fig. 7. Temperature distribution in developing flow with $k_{th}, k_{pl} = 1k_a$ for $B/W = 0.2$ and $Re = 1000$.

the Reynolds number reaches 1000, the circulating flow covers the entire cavity with the main stream passing over the cavity, as seen in Fig. 4(B). At $Re = 1000$, flow circulation in the first cavity is stronger than that in the ninth cavity, while little difference is observed at $Re = 100$. This is because after undergoing a large deflection induced at the first block, the flow tends to slide over the cavity downstream of the first block. This also implies that the hydrodynamic entrance region length at $Re = 1000$ is much longer than that at $Re = 100$.

Transverse velocity profiles at the middle of the cavities are examined at $Re = 100$ and 1000 for the blocks with $B/W = 0.2$ and 0.4. The channel width, D, is the same as the block width, W, while the block pitch, P, is twice as the block width, $2W$. Only the transverse velocity profiles for $B/W = 0.2$ are presented in Fig. 5 for both developing flow and the periodically fully developed flow for comparison. The figure shows the transverse velocity profiles at the cavities 1, 5, and 9 and velocity profile of periodically fully developed flow with the velocities being normalized with the bulk velocity V_b. As can be seen from the figure, the transverse velocity profiles of all cavities in the developing flow practically coincide with that of periodically fully developed flow. This implies that the developing flow has practically reached a periodically fully developed state at its second module. However, this is not the case at the higher Reynolds number, $Re = 1000$. The developing flow velocity profiles fail to come to close to that of periodically fully developed flow even at its ninth cavity. This observation is in accord with the fact that the entrance region length increases with the Reynolds number. Similar phenomena are observed for $B/W = 0.4$ case. In laminar flow, the hydrodynamic entrance length can be approximated by the form [14]

$$L_{fd,h} \approx 0.05 Re_{Dh} D_h \tag{27}$$

Here, the Reynolds number is based on the hydraulic diameter of the channel, D_h. Using Eq. (27), the entrance length of this channel flow reaches $100D$ at $Re = 1000$. Therefore, when the block pitch, P, is $2W$, the flow would reach a fully developed flow state at around the 50th blocks.

Fig. 6 displays the variation of friction factors along the blocks for $B/W = 0.2$ and 0.4. The corresponding friction factor for periodically fully developed flow shown at the block number 11 is superimposed for comparison. In both flows, the friction factor f falls substantially from the first to second blocks due to the abrupt change in the flow direction as seen in Fig. 3(a). The friction factor recovers as the flow reaches the third block and takes a fairly constant value thereafter. It is observed that the f curve drops with an increase in the Reynolds number Re, indicating the benefit of higher coolant flow.

4.2. Heat transfer performance

Fig. 7 depicts temperature distribution in a developing flow through the channel at $Re = 1000$. Coolant air enters with uniform temperature 20 °C at $y/W = 0$. Both $k_{b,th}$ and $k_{b,pl}$ are $1k_a$. Nearly symmetrical, cone-shaped isotherms such as 25, 30, 35 and 40 °C are formed with the axis located at the center of the flow passage between the block tips and the plane board (without block). The effect of convection–conduction conjugate mode in both the boards with and without the blocks is clearly visible through the unusual distribution of the isotherms in the coolant near the plane board. The magnitude of isotherms in and around the blocks increases in the downstream direction, from the first to the last (10th) blocks. This isotherm distribution pattern constitutes the basic mechanism for the distribution pattern of both the local and average heat transfer coefficients in the system.

Thermal performance of a developing channel flow is investigated to determine when the flow reaches a thermally fully developed state. The distribution of local

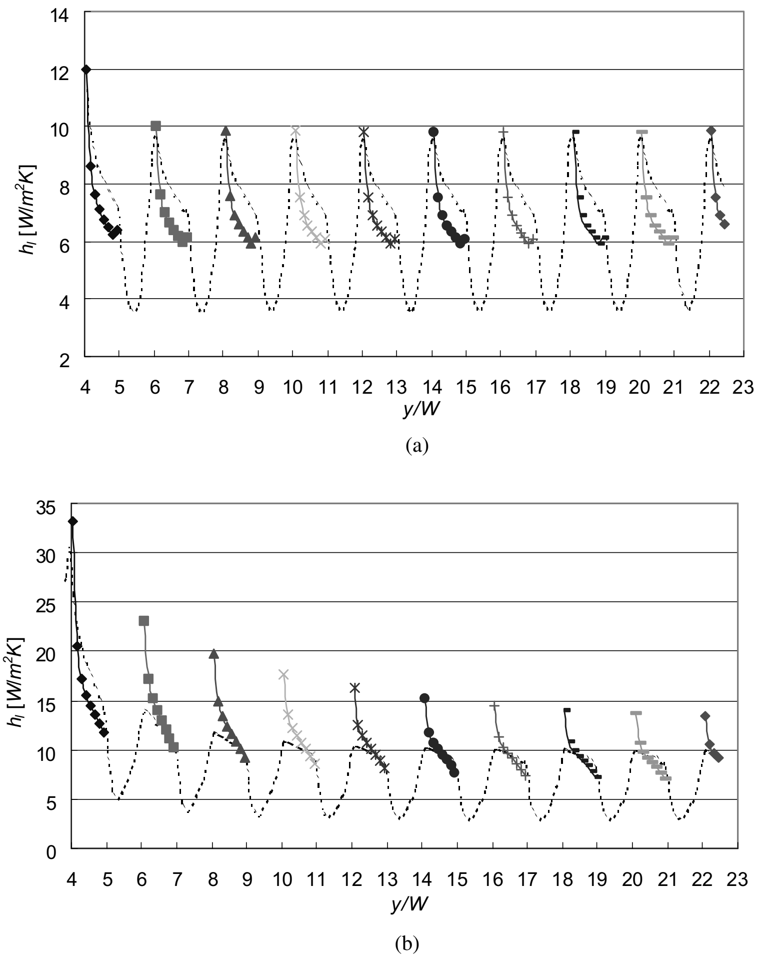


Fig. 8. Variation of local heat transfer coefficient for $B/W = 0.2$, $R_{cb} = 0.01$ and $k_{b,th} = k_{b,pl} = k_a$ (solid lines for block surface and broken line for upper board surface): (a) $Re = 100$ and (b) $Re = 1000$.

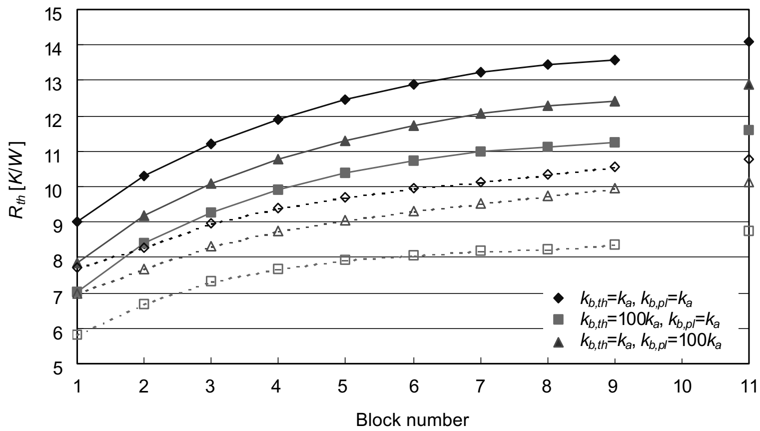
heat transfer coefficients on both the block top surface and upper board surface in the stream-wise direction is presented in Fig. 8 for $B/W = 0.2$. R_{cb} is 0.01 (K m^2/W) and the board is uniform conductivity k_a in all results of the figures. The solid line indicates the local heat transfer coefficient along the block surface and the broken line indicates that along the upper board surface. It is seen that at a low Reynolds number of 100, the periodic variation of the local heat transfer coefficients is achieved on both the block top and upper board surfaces at the second module with y/W between 6 and 7. However, at a high Reynolds number of 1000, the periodicity is gradually established towards the last block, without a distinct location for the inception of a thermally fully developed state.

It is observed in Fig. 8 that periodic thermal behavior in the flow direction is induced by periodic heating due to block heating. Each cycle begins with a maximum and follows a "v" shape curve, as illustrated by the broken line. The maximum local heat transfer coefficient occurs at the upstream edge of each heating block caused by an upsurge in the flow velocity, as observed at $y/W = 4.0$ in Fig. 3(a) and at $y/W = 6.0$ and 22.0 in Fig. 4(A) and (B). The heat transfer performance diminishes gradually along the heating block surface, followed a dip and subsequent recovery, thus forming a valley, during a cavity flow as seen in Fig. 4(A) and (B).

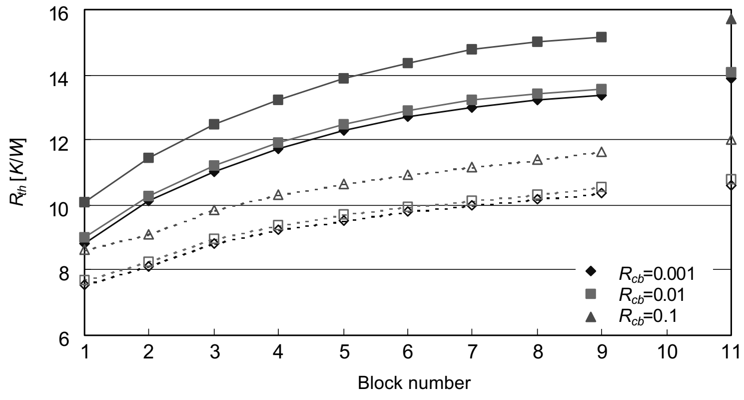
Thermal performance in an electronics chip cooling is often examined in terms of thermal resistance between the chip junction and the cooling medium. The Nusselt number of a channel is a good indicator for examining the thermal performance in a channel flow. However, heat transfer in electronics cooling is a combination of convection in channel air flow and conduction of printed circuit board and chip module, a sort of conjugate heat transfer problem. Therefore, the thermal resistance between the chip module and the channel bulk flow, defined in Eq. (26), is a better choice for examining the thermal performance in electronics chip cooling.

The variation of thermal resistances in the stream-wise direction are presented in Fig. 9(a) and (b) for the various board conductivities and case-to-base thermal resistances, respectively. R_{cb} is fixed to be 0.01 [K m^2/W] in Fig. 9(a) and the board is uniform conductivity k_a in Fig. 9(b).The corresponding thermal resistances of periodically fully developed flow are superimposed at the block number 11 for comparison. Results of two different block height, $B/W = 0.2$ and 0.4 are shown in the same figures. At a low Reynolds number of 100 (not shown), the thermal resistance after the second block remains constant at its corresponding values for periodically fully developed flow. Hence, one can conclude that the flow has reached a thermally fully developed state at the second module. At a high Reynolds number of 1000, the thermal resistance approaches to its periodically fully developed value, as the flow proceeds downstream, i.e., as the block number increases. However, this trend continues until the ninth block. Therefore, the flow has not reached its thermally fully developed state even at the ninth block.

The interesting result is attributed to non-uniform thermal conductivity of the board, due to non-homogeneity of printed circuit board. An increase in the conductivity through the board thickness, $k_{b,th}$, has more effect on reducing the chip-to-bulk flow thermal resistance than an increase in the in-plane thermal conductivity, $k_{b,pl}$. This implies that an increase in the conductivity through the board thickness would contribute more to thermal performance of chip cooling than an increase in the in-plane conductivity of the board. This result suggested the remedy for low thermal conductivity by installing thermal vias or heat slug in a layered printed circuit board under a chip. In general,



(a)



(b)

Fig. 9. Variation of thermal resistances in the stream-wise direction with the result of periodically fully developed flow (solid line for $B/W = 0.2$ and broken line for $B/W = 0.4$): (a) various board conductivities at $R_{cb} = 0.01$ and (b) various case-to-base thermal contact resistance with $k_{b,th} = k_{b,pl} = k_a$.

an increase of the thermal contact resistance leads to the increase of the junction temperature. In Fig. 9(b), the considerable increase of R_{th} is observed between $R_{cb} = 0.1$ and 0.01 in all results. The air gap between the chip case and board Δx_a is calculated using Eq. (24). For $R_{cb} = 0.01$, the calculation yields $\Delta x_a = 0.28$ mm. This might suggest that the air gap between the chip case and board should be designed not to exceed 0.28 mm.

5. Conclusions

A method has been developed to numerically investigate thermal-fluid flow behavior in a bundle of parallel boards with heat producing blocks. The system simulates cooling passages in a stack of electronic circuit boards with heat generating chips. Numerical results have been obtained for velocity vectors, isotherms, friction factor, local and average heat transfer coefficients, and thermal resistance. It is disclosed that at a low Reynolds number flow, a developing flow may achieve a fully developed flow state at certain block number from the entrance. However, the block number for a flow to become fully developed increases with an increase in *Re*. At low *Re*, a circulation is developed inside the separation regime in each cavity with the main stream dip into the downstream region of the cavity. However, at high *Re*, the circulating flow occupies on entire cavity with the main stream travels straight over the cavity. Those flow patterns constitutes the basic mechanisms of behavior of local heat transfer coefficients and eventually that of average heat transfer coefficient. Both the fluid flow and heat transfer performance resembles those in ribbed channel flow.

An increase in the conductivity through the board thickness had more effect on reducing the chip-to-bulk flow thermal resistance than by an increase in the in-plane thermal conductivity. This result suggests the remedy for low thermal conductivity by installing thermal vias or heat slug in a layered printed circuit board under a chip. It was also discovered that the air gap between the chip case and the board had a considerable impact on the junction temperature. It is important to model the case-to-board thermal contact resistance R_{cb} to determine the correct junction temperature.

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